IN THE CLAIMS:

Please amend claims 1-6 as follows.

1. (Currently Amended) Method for controlling a phase locked loop during change of synchronisation source, in which method

- ~~the~~ a synchronisation signal is changed from a first synchronisation to a second synchronisation signal,

- ~~the~~ a phase difference between ~~the~~ said second synchronisation signal and a signal formed from ~~the~~ a phase lock's oscillator is measured,

- the phase difference between the second synchronisation signal and the signal formed from the phase lock's oscillator is changed, if ~~the~~ a measured phase difference is greater than a predetermined limit value, whereupon the phase difference between ~~the~~ said second synchronisation signal and the signal formed from the phase lock's oscillator is again measured,

- the phase locked loop's normal adjustment function is started, when the measured phase difference is less than or equal to ~~the said~~ a limit value,

wherein

in response to ~~the~~ a finding, that ~~the~~ said phase difference is less than or equal to ~~the~~ said limit value, the measured phase difference is set as ~~the~~ a setting value for the phase difference for the normal adjustment function of the phase locked loop, whereupon the adjustment function is started.

2. (Currently Amended) Method as defined in Claim 1, wherein phase transfer of the second synchronisation signal is carried out by preventing for a certain time access of the signal formed from the phase lock's oscillator to ~~the~~ a component measuring the phase difference of the phase locked loop.

3. (Currently Amended) Method as defined in Claim 2, wherein preventing takes place by cutting off ~~the~~ a functional route of the signal formed from the oscillator to the component measuring the phase difference of the phase locked loop.

4. (Currently Amended) Method as defined in Claim 2, wherein preventing takes place by cutting off ~~the~~ a functional route of the second synchronisation signal to the component measuring the phase difference of the phase locked loop.

5. (Currently Amended) Digital phase lock arrangement, which includes,

- selection components for selecting ~~the~~ a desired synchronisation source from a set of at least two different synchronisation sources,

- a phase comparator, which has a first and a second input and which is used for generating an output signal dependent on ~~the~~ a phase difference between ~~the~~ signals supplied to the inputs,

- controllers for forming a control word in response to ~~the said~~ an output signal which is dependent on the phase difference, and

- an oscillator, which is controlled with the aid of ~~the~~ said control word,

wherein

~~the~~ said controllers also include setting components for setting ~~the~~ a measured phase difference as a setting value for ~~the~~ a normal adjustment function of ~~the~~ a phase lock.

6. (Currently Amended) Arrangement as defined in Claim 4, which includes starting components for starting the normal adjustment function of the loop,

wherein ~~the~~ said starting components respond to the setting components in order to start the adjustment function in response to ~~the~~ a setting of a setting value.